Pixel Structure with 10 nsec Fully Charge Transfer Time for the 20M Frame Per Second Burst CMOS Image Sensor

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ABSTRACT

In this paper, we demonstrate the technologies related to the pixel structure achieving the fully charge transfer time of less than 10 nsec for the 20M frame per second burst CMOS image sensor. In this image sensor, the size of the photodiode (PD) is 30.0 $\mu m^H \times 21.3\ \mu m^V$ in the 32.0 $\mu m^H \times 32.0\ \mu m^V$ pixel. In the pixel, the floating diffusion (FD) and the transfer-gate-electrode (TG) are placed at the bottom center of the PD. The n-layer for the PD consists of the semicircular regions centered on the FD and the sector-shaped portions extending from the edges of the semicircular regions. To generate an electric field greater than the average of 400 V/cm toward the FD direction in the entire PD region, the n-layer width of the sector-shaped portions becomes narrower from the proximal-end to the distal-end. By using the PD structure, which includes the above mentioned n-layer shape and the PD dopant profile with the condition of three times n-type dopant implantation, we achieved to collect 96 % of the charges generated in the PD at the FD within 10 nsec. An ultra-high speed CMOS image sensor with the abovementioned pixel structure has been fabricated. Through the experiments, we confirmed three key characteristics as follows; the image lag was below the measurement limit, the electron transit time in the PD was less than 10 nsec, and the entire PD region had equivalent sensitivity.

Keywords: burst CMOS image sensor, ultra-high speed, pixel structure, fully charge transfer

1. INTRODUCTION

In engineering, science and biological fields, ultra-high speed (UHS) video cameras are widely used in order to dynamically and accurately analyze the physical phenomena such as combustion, materials fracture, and electric discharge. Recently, there is a strong demand for UHS cameras of which maximum frame rate is over 1M frame per second (fps) [1].

There are five factors which limit the readout speed [2-3]. (I) Settling time for the pixel drive signals. (II) Transit time of photo-electrons in the large photodiode (PD). (III) Readout time from the pixel to the column line. (IV) Signal processing time in the column circuits. (V) Readout time from the column circuits to the chip output. In this paper, we demonstrate a developed pixel structure which improves the factor (II).

In the field of UHS imaging, especially high frame rate and high sensitivity are required. Fig. 1 shows the requirements for the pixel of the UHS image sensors. The requirements are summarized as follows. To increase the number of generated charges, (1) enlarging the size of the PD is necessary. To increase the charge collection efficiency, (2) enlarging the size of the n-layer (charge integration) region is required. In this paper, we define the charge collection efficiency as the proportion of the charges collected in the floating diffusion (FD) to all charges generated in the PD. The charge collection efficiency is determined by the products of the proportion of the charges collected in the n-layer to all charges generated in the PD and the proportion of the charges collected in the FD within an intended time to the charges collected in the n-layer. To improve the conversion gain (C.G.), (3) minimizing the capacitance of the FD is required if the charge-voltage conversion process is carried out in pixels. When the PD size is enlarged, it becomes more difficult to collect all of the generated charges in a short time. Therefore, (4) generating an electric field is necessary, toward the FD in the CMOS image sensor case or the charge collection gate in the CCD case.

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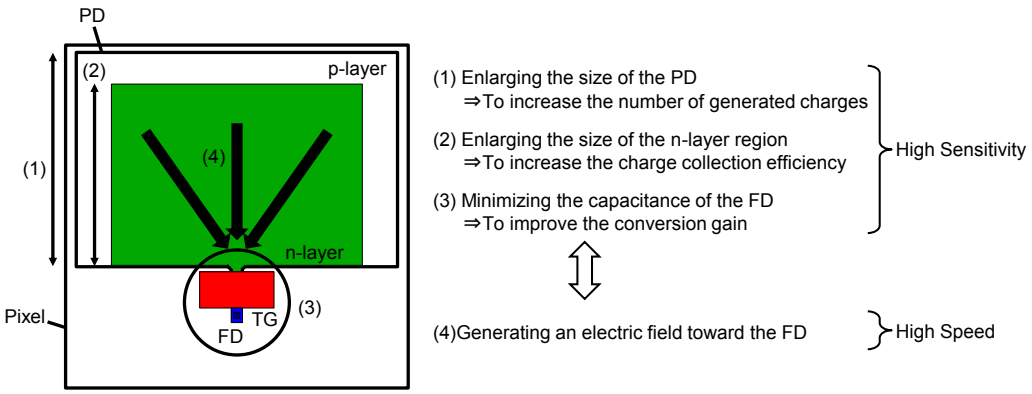


Figure 1. Requirements for the pixel structure of the UHS image sensors. The figure shows an example of the CMOS image sensor case.

To achieve 20M fps burst video operation, the transit time from the PD to the FD is to be only 10 nsec or less. Therefore, in order to increase the charge collection efficiency, it is necessary to generate an electric field in the PD toward the FD.

Some approaches that generate an electric field in the PD toward the FD have been reported. The first approach is to design the n-layer shape of the PD in order to generate an electric field by using a difference of pinned voltage [4-7]. By using this approach, it is possible to generate an electric field toward the FD without extra processes, however, the n-layer region tends to be small because n-layer must be sandwiched by p-type regions. The second approach is to control the n-layer dopant concentration [8-10]. By using this approach, it is possible both to enlarge the n-layer region and to create an electric field toward the FD, however, some additional photomasks or extra processes are necessary.

In this paper, we demonstrate the 30.0 $\mu m^H \times 21.3\ \mu m^V$ PD achieving the fully charge transfer time of less than 10 nsec using a minimum number of photomasks without extra processes to the standard CMOS image sensor process. In section 2, we summarize the design of the pixel structure of CMOS image sensor for UHS video cameras. In this image sensor, in order to increase the charge collection efficiency, we generate a constant electric field toward the FD in the entire PD region by both controlling the dopant concentration and optimizing the width of the n-layer. In section 3, we introduce the following measurement results. In order to confirm that it is possible to collect in the FD all charges generated in the PD within 10 nsec, we measure the image lag, electron transit time in the PD and the sensitivity distribution in the PD. In addition, we measure spectral sensitivity.

2. DESIGN OF THE PIXEL STRUCTURE

2.1 Overview of the FTCMOS image sensor [11-12]

For the UHS cameras, improvements of frame rate, the number of pixels, the number of record length are simultaneously required. The UHS cameras using burst image sensors including multiple on-chip memories for each pixel are the closest to meet all of the requirements. In this type of the image sensors, the capturing images are temporarily stored in the on-chip memories provided for each pixel to separate the image capture and the signal output operations. Therefore, (V) readout time from the pixel to the column line mentioned in the previous section does not limit the readout speed. An image sensor with the linear CCD connected to each PD [4, 13] and an image sensor with two-dimensional 180 CCD memories placed in each pixel [7, 14] have been reported. These image sensors achieve over 1M fps, however, there are issues such as a difficulty to increase the number of record length, high power consumption and heat generation. The main reason of high power consumption and heat generation is that these image sensors have to drive all connected CCD memories during the charge transfer operation.

We developed the 20M fps burst CMOS image sensor; FTCMOS [11-12]. The block diagram of this image sensor and one parallel unit from the pixel to the output circuit are shown in Fig. 2(a). It has a pixel array, two on-chip memory arrays placed on top and bottom of the pixel array, vertical scanning circuits, 20 × 2 parallel horizontal scanning circuits and output circuits. The pixel array region and the on-chip memory arrays region are spatially separated so as to allow us to

independently design both the pixel and the on-chip memory layouts. The power consumption and heat generation of this image sensor is lower than those of the conventional burst CCD image sensors. It is because this CMOS image sensor drives only the corresponding memories that capture signals in each frame. In addition, the parasitic capacitance and resistances of the pixel pulse wires and pixel output wires of this CMOS image sensor are much smaller than those of the burst CCD image sensors. In order to realize high readout speed from pixel to on-chip memories, multiple pixel output wires are placed in each pixel column. Fig. 2(b) depicts the equivalent circuit of the pixel. The 32.0 μm^H × 32.0 μm^V pixel has a large pinned PD, a charge transfer switch (TG), a FD to convert charge to voltage, a reset switch (R), source follower amplifiers (SF1, SF2), pixel select switches (X1, X2), current source transistors (CS1, CS2), and a noise reduction circuit. This FTCMOS image sensor operates in two types of modes as follows. One is the full resolution operation using 100K pixels with 128 burst video operating frames and the maximum frame rate of 10M fps. The other is the half resolution operation using checker-pattern 50K pixels with 256 burst video operating frames and the maximum frame rate of 20M fps. Fig. 2(c) shows the timing of the pixel pulses. There are three factors that limit the readout speed. (I) Settling time for the pixel drive signals. (II) Transit time of photo-electrons in the large PD. (III) Readout time from the pixel to the on-chip memory. There are some technologies implemented in this image sensor to solve these speed limitation issues. In order to reduce the parasitic resistance and capacitance, the CMOS process is used in this image sensor. In order to improve the readout speed, each column features multiple pixel output wires and source follower buffers are placed on the pixel output wires between the pixels and on-chip memories. In this paper, we introduce the technologies to solve the factor (II) in detail.

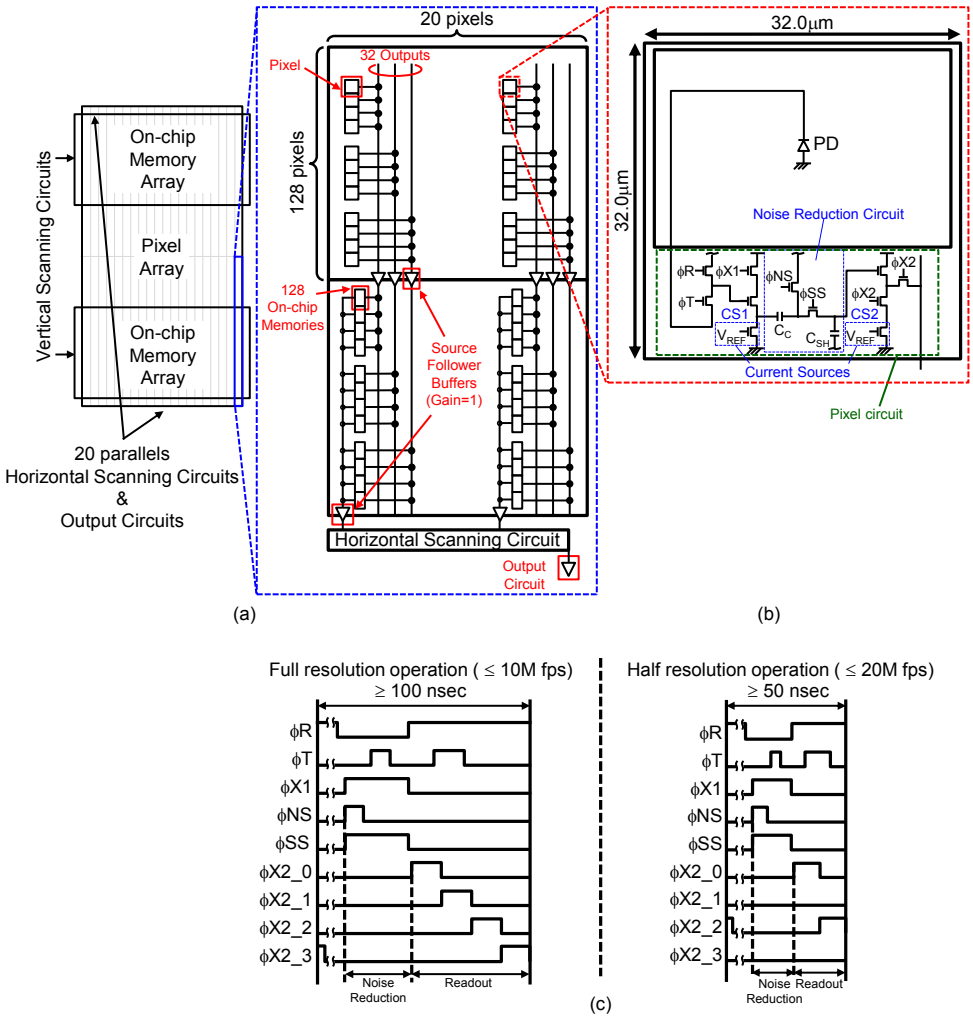


Figure 2. The structure of FTCMOS image sensor [11-12]. (a) Block diagram, (b) pixel structure, and (c) timing diagram of the pixel pulses.

2.2 Photodiode Concept

In order to create an electric field in the PD, we optimize the design of the n-layer shapes of the PD as follow. Taking an example, we simulated the potentials of the n-layer. In this simulation [15], we took account of the impurity concentration of the depth direction as well as the lateral direction. From the result, the relation between the n-layer width and the highest potential in the n-layer is shown in Fig. 3(a). Fig. 3(b) shows the n-layer of the PD to create an electric field in the PD. The width of the n-layer of the PD is optimized from the proximal-end to the distal-end based on the function of Fig. 3(a). Fig. 3(c) shows the cross sectional potential of Y-Y' in Fig. 3(b). It is confirmed that there is a constant electric field in the n-layer of the PD.

In this image sensor, in order to increase the charge collection efficiency, we generate a constant electric field toward the FD in the entire PD region by both controlling the dopant concentration and optimizing the width of the n-layer. Fig. 4 shows several PD shapes. In these all shapes, electron transit time from the corner of the PD to the FD is less than 10 nsec. Only controlling the dopant concentration (Shape (a)), only optimizing the width of the n-layer (Shape (b)), combination of controlling the dopant concentration and optimizing the width of the n-layer (Shape (c) and (d)). Shape (c) is a shape of which size of concentration gradient formation region is large. On the other hand, shape (d) is a shape of which size of concentration gradient formation region is smaller than shape (c). Shape (d) is superior in terms of the size of the n-layer and the simplicity of the process. Shape (d) shows the n-layer shape, which has the high doping concentration level of the near FD region, and the low doping concentration level of the far FD region with the doping condition of three times n-implantation. In addition, there are sector-shaped potions extending the edges of the semicircular regions. From the simulation results, we are not able to achieve enough area of the n-layer with the condition of two times n-implantation. On the other hand, even with the condition of more than equal to four times n-implantation, the area of the n-layer is not so different from that with the condition of three times n-implantation. Therefore, in this size of the PD, three times n-implantation was employed.

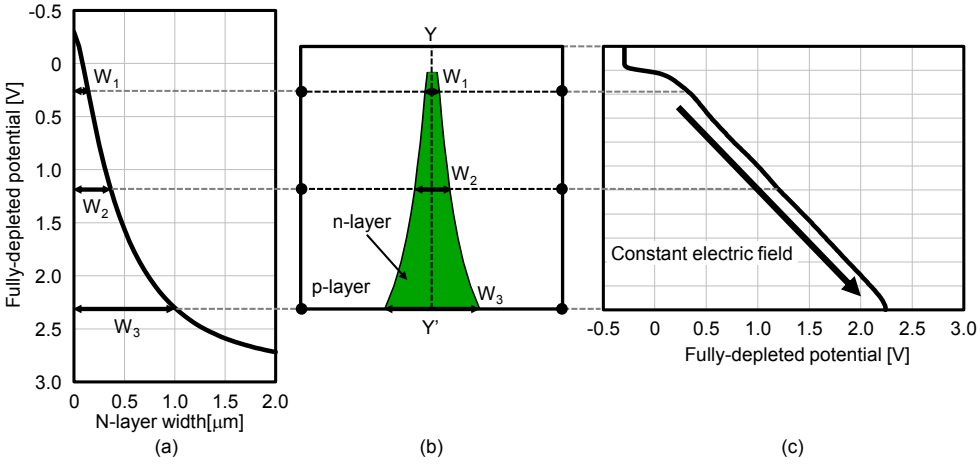


Figure 3. The relation between the n-layer width and the fully depleted potential in the n-layer, (a) simulation result of fully depleted potential of the n-layer, (b) the plane view of the sector-shaped potion to generate a constant electric field, and (c) cross sectional potential of Y-Y' in (b).

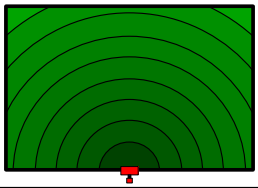
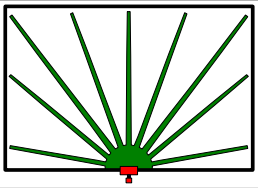
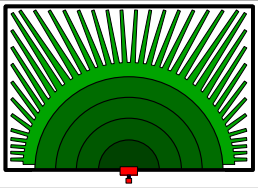
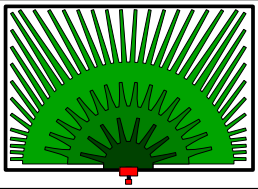
	Shape(a)	Shape(b)	Shape(c)	Shape(d)
n-layer Layout				
n-layer region	✓Large	Small	✓Large	✓Large
Process	Not simple	✓Simple	Not simple	✓Simple

Figure 4. Comparison of the PD structures.

2.3 Design of the n-layer

In this sub-section, we introduce the design of the n-layer of the PD. In this pixel structure, the FD and the TG are placed at the bottom center of the PD in order to minimize the capacitance of the FD. The PD size is 30.0 $\mu m^H \times 21.3\ \mu m^V$, therefore, the longest path from the edge of the PD to the FD is about 25 μm. In order to achieve electron transit time less than 10 nsec in 25 μm, an electric field greater than average of 400 V/cm toward the FD is required. We make this electric field by using a combination of controlling n-layer shape and concentration control of the n-layer based on the concept explained in Fig. 4(d).

Figure 5 shows the plane view and the cross sectional view of the designed PD. In order to collect charges from the entire PD region, the n-layer of the PD consists of the semicircular regions centered on the FD and the sector-shaped portions extending from the edges of the semicircular regions. In each part of the sector-shaped portions, the width of the n-layer of the PD becomes narrower from the proximal-end to the distal-end like Fig. 3(b) to generate a constant electric field toward the FD direction. The sector-shaped portions were placed as many as possible so as to enlarge the areas of n-layer region. We designed three n-layer regions (N_1, N_2 and N_3) based on the abovementioned n-layer shape. The closest n-layer region to the FD is N_1, and the most distant n-layer region from the FD is N_3, and the N_2 is located between N_1 and N_3. Each n-layer region has different doping concentration and different radius of the semicircular region. The n-layer doping concentration level of the N_1 is the highest and that of the N_3 is the lowest. In order to suppress the effect of fluctuation process, N_3 region covers N_2 and N_1 region, likewise N_2 region covers N_1 region, respectively. The potential at N_1 is the highest and that at N_3 is the lowest. The lengths of the sector-shaped portions in the N_3 region are longer than those in the other n-layer regions. As a result, the shape of n-layer looks like a Japanese fan.

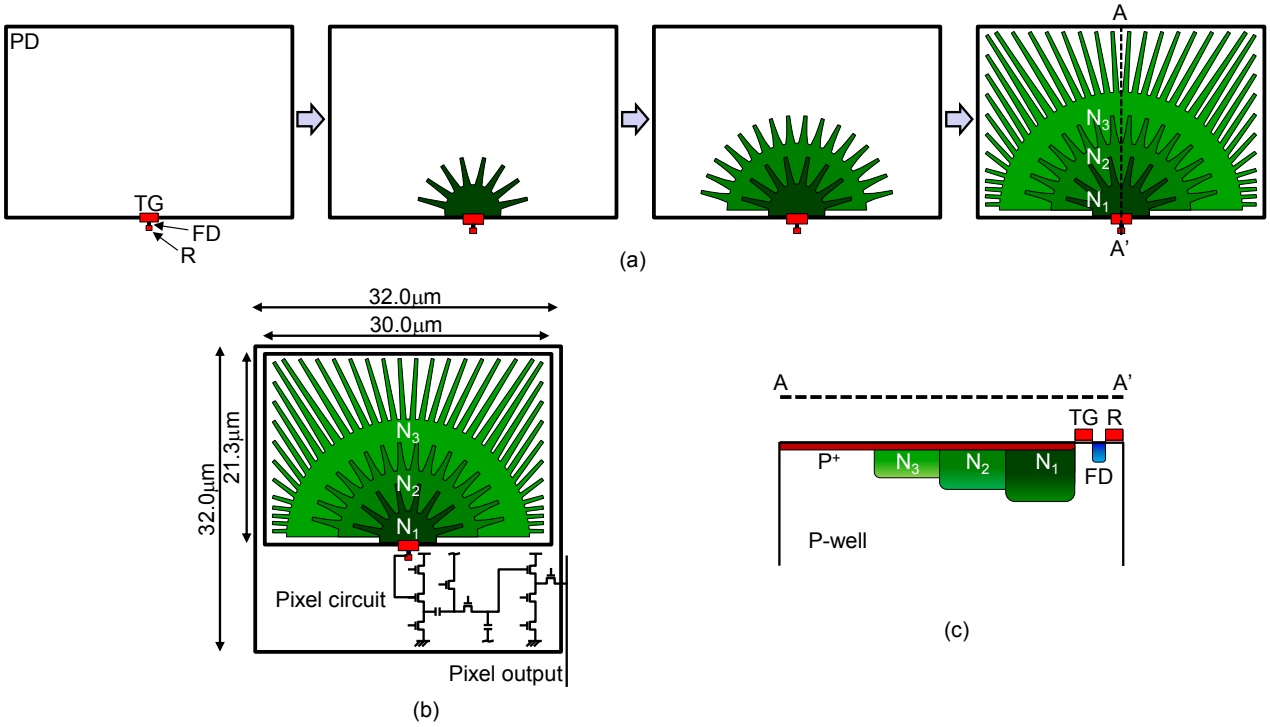


Figure 5. The designed PD shapes of this UHS image sensor. (a) Plane view, (b) PD and pixel structure, and (c) cross sectional structure of A-A' shown in (a).

2.4 Simulation result of charge transfer

Figure 6 shows the simulation results of the electron transit time of a charge generated at the three points of the PD (A, B, C). The electron transit path and the cross sectional potential from the bottom left, from the upper left, and from the upper center of the PD to the FD are shown in Figs. 6(a-c), respectively. From the simulation results, we confirmed that wherever a charge was generated in the PD, the electron transit time to the FD was less than 10 nsec. In addition, we calculated the charge collection efficiency through the transient analysis, under the light condition that all PD region was exposed. From the simulation, the proportion of the charges collected in the n-layer regions to the charges generated in the PD was 96 %. The proportion of the charges collected in the FD within 10 nsec to the charges collected in the n-layer region was 99.99 %. Therefore, charge collection efficiency, which is determined by the products of those two factors, was 96 %. The charges not collected in the n-layer moved to the n-substrate, therefore, those charges do not cause the image lag.

2.5 Specification of the fabricated chip

Figure 7 shows the chip micrograph and Table 1 shows the specification of this fabricated chip. Die size, pixel size, PD size, the number of pads, and the number of pixels are pin-compatible with the previously reported one [11-12]. Meanwhile, we improve the peripheral circuit designs and decrease the power-supply voltage.

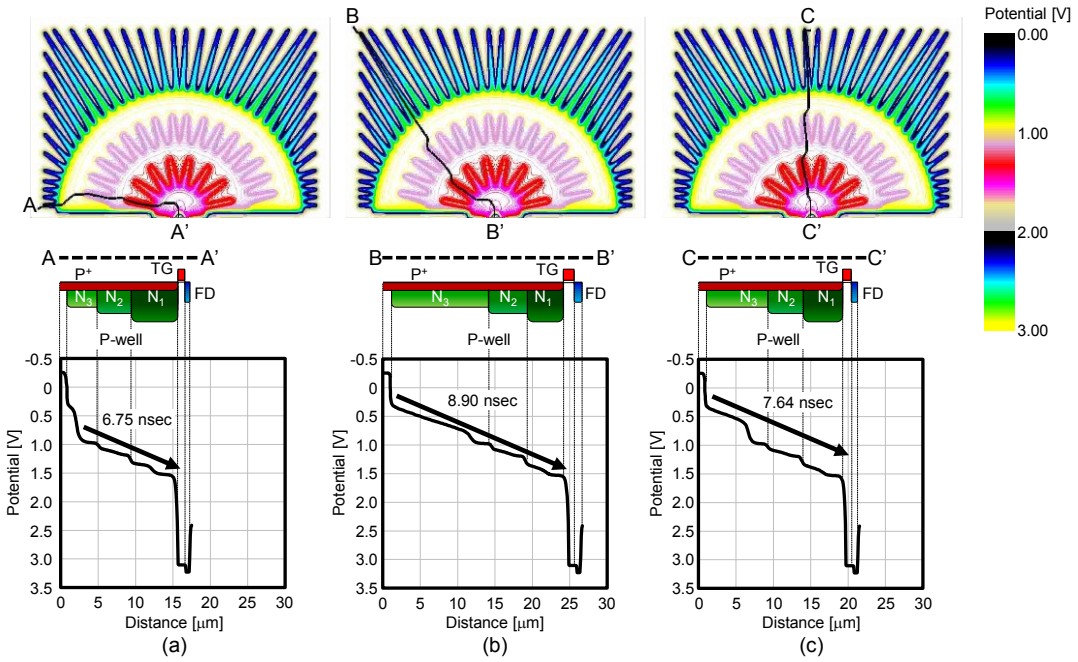


Figure 6. The distribution of the potentials in the electron transit path (a) A-A', (b) B-B', and (c) C-C'.

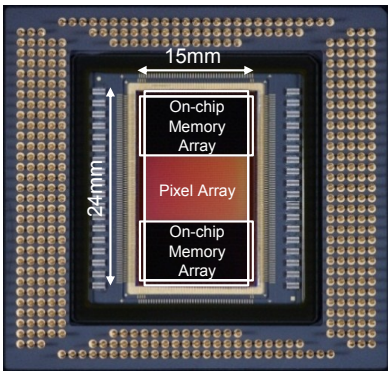


Figure 7. Chip micrograph of the fabricated chip.

Die Size	15 mm^H × 24 mm^V
Pixel Size	32.0 μm^H × 32.0 μm^V
PD Size	30.0 μm^H × 21.3 μm^V
# of Pads	424
# of Pixels	400 ^{H} × 256 ^{V} (Effective 400 ^{H} × 250 ^{V})
Power Supply	3.3V
PD Structure	・With a constant electric field toward the FD by both controlling the dopant concentration and optimizing the width of the n-layer. ・Three times n implantation is employed. ・With UV sensitivity.

Table 1. Summary of the specification of the fabricated chip.

3. EXPERIMENTAL SETUP AND RESULTS

3.1 Image lag

Figure 8(a) shows the measurement system of the image lag. The light source was the 635 nm laser-diode (LD). In order to fine-tune the point of the light source, the LD light source was set on the XYZ stage. Additionally, the XYZ stage and the UHS camera were on the same anti-vibration table. The LD light source was synchronized with the UHS camera in order to adjust the timing of the light exposure and the driving pulses of the fabricated chip. Fig. 8(b) shows the pulse timing to measure the image lag. By using this pulse timing, we are able to capture images at 20M fps burst half resolution video operation. The UHS camera was exposed to the LD light source during only the frame number of 0. Fig. 8(c) shows the captured images of this experiment. The LD light was confirmed only in the frame number of 0. In order to calculate the image lag, output signals of 30 pixels were extracted of which output intensities were the highest at the frame number of 0. The image lag was determined as the ratio of the average of those pixels output values in the each frame to that of the frame number of 0. Fig. 8(d) shows the measurement result of the image lag. We confirmed that the image lag after the frame number of 1 were less than the measurement limit. From this result, the image lag was not detected in the fabricated chip during 20M fps burst half resolution video operation.

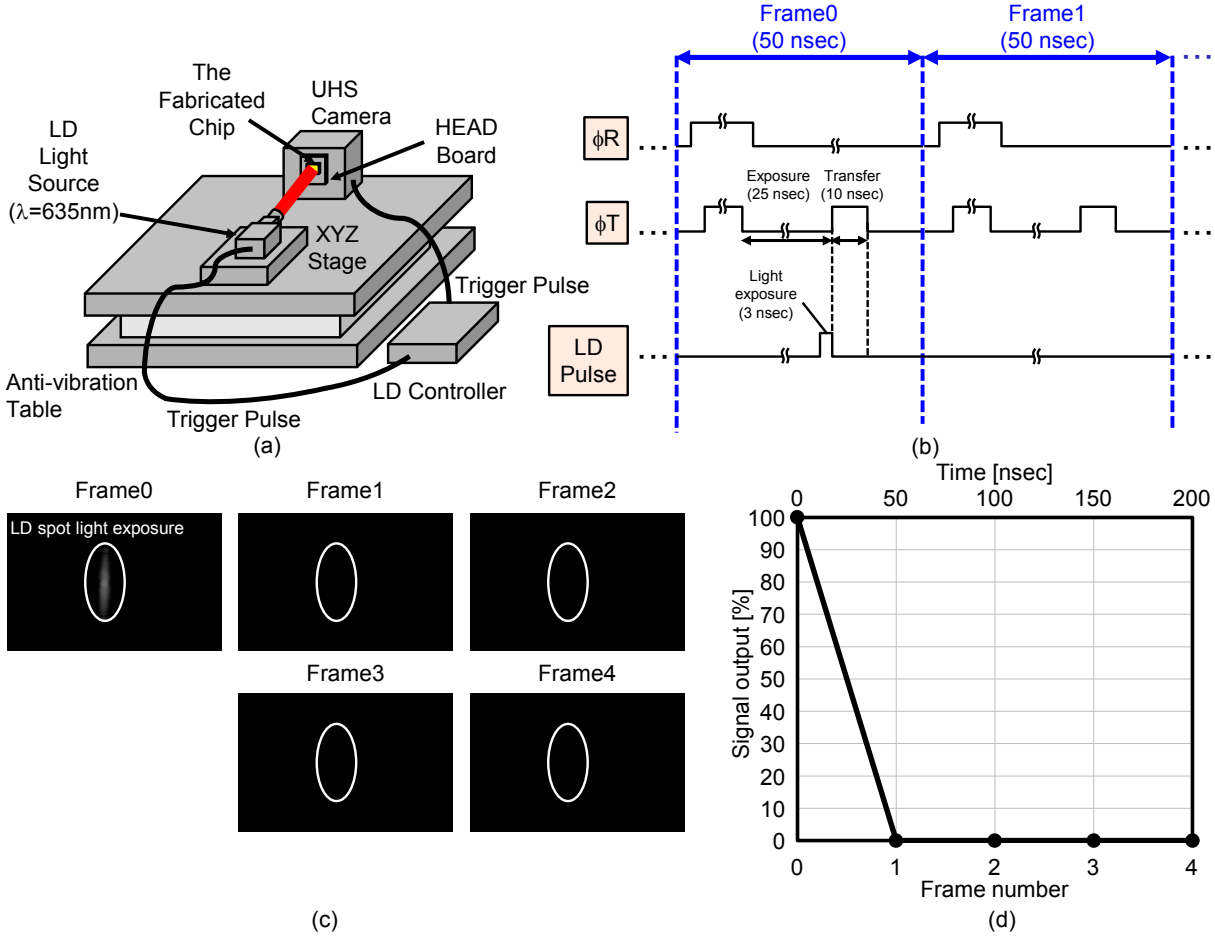


Figure 8. The measurement system and result of image lag. (a) Measurement system, (b) pulse timing, and (c) (d) the measurement results.

3.2 The electron transit time in the PD

Figure 9 shows the measurement system and results of the evaluation of the electron transit time from the PD to the FD. Fig. 9(a) shows the measurement system. In order to focus the LD light diameter into about 5 μm on the light receiving surface, the LD light source was set on one side of the eyepieces of the microscope. The monitor camera was set on the other side of the eyepieces to identify the place exposed to the LD light. In order to fine-tune the area exposed to the LD light, the fabricated chip on the head board was set on the XYZ stage. Fig. 9(b) shows the positions exposed to the LD light, and Fig. 9(c) shows the pulse timing for this experiment. The number of positions exposed to the LD light was five, and the transfer time (T_{trans}), determined as the time span from turning on LD pulse to turning off ϕT, was changed from -5 nsec to 20 nsec by 1 nsec. Fig. 9(d) shows the measurement result of this experiment. The horizontal axis is T_{trans} and the vertical axis is the signal output. The plots from A to E correspond to the areas exposed to the LD light shown in Fig. 9(b) respectively. The time lags from A to C, D, and E were 2.5 nsec, 3.0nsec, 5.0 nsec respectively. From the results, electron transit time in the PD was about 5 nsec.

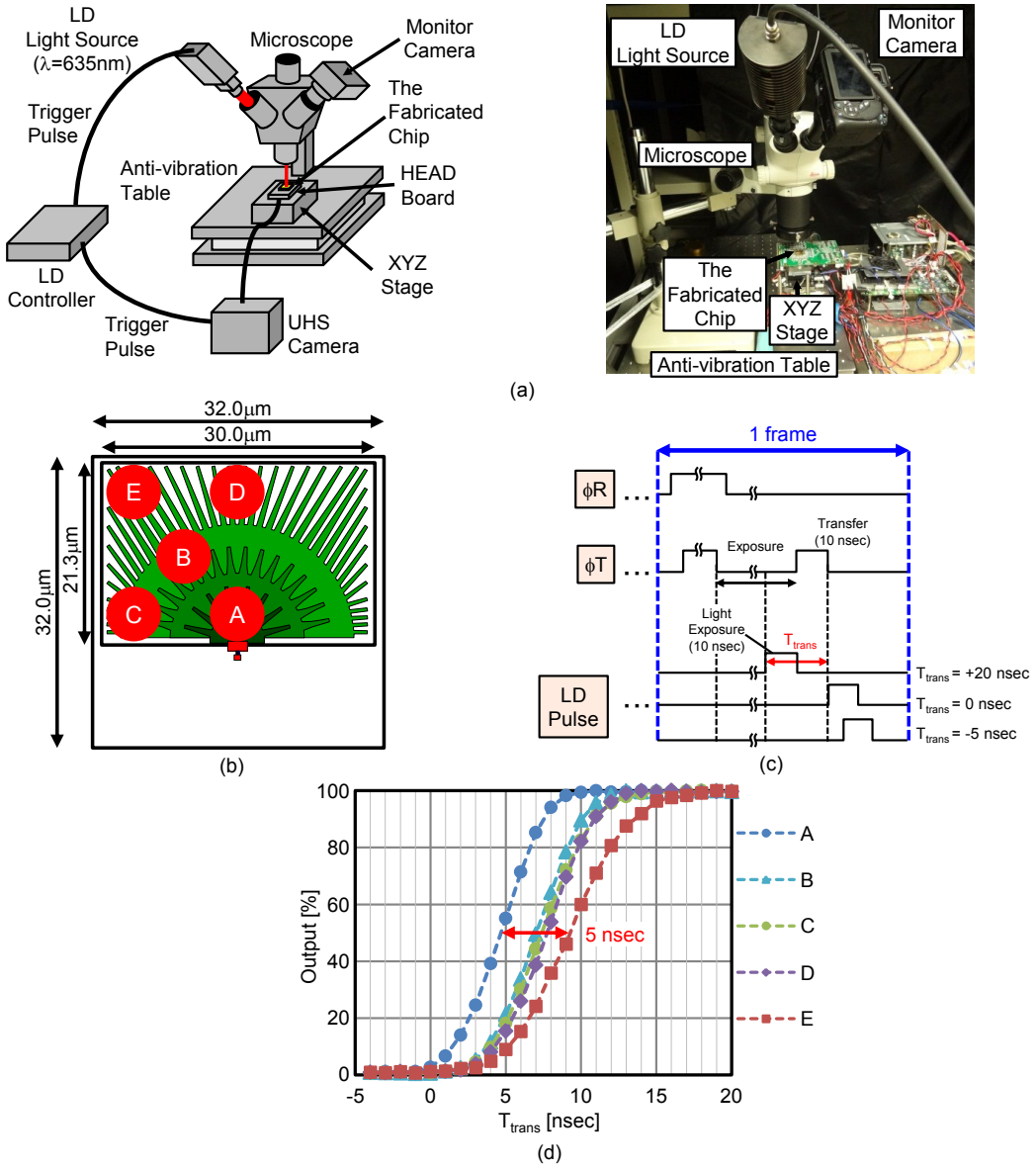


Figure 9. The measurement system and result of electrons transit time in the PD. (a) Measurement system, (b) The LD light exposure spot in the PD, (c) pulse timings, and (e) measurement result.

3.3 The sensitivity distribution in the PD

Figure 10 shows the measurement system and the result of the sensitivity distribution in the PD. Fig. 10(a) shows the measurement system. The light source was set in front of the fabricated chip, a photomask and the lens were set between the light source and the fabricated chip. The photomask had two-dimensional array of holes to make the spotlight on the fabricated chip. The pitch of the spotlight was adjusted to be slightly wider than the pixel pitch on the fabricated chip. Fig. 10(b) shows the example of the surface of the fabricated chip with light exposure. If the entire PD region has the same sensitivity, the output image becomes like Fig. 10(c). If there are positions with small sensitivity in the PD, the output image becomes like Fig. 10(d). Fig. 10(e) shows the measurement result. The PD shape in the pixel was clearly confirmed in the image. We confirmed that there was the same output value in all pixels of which the PD was exposed. Therefore, we confirmed that the entire PD region of this pixel had equivalent sensitivity.

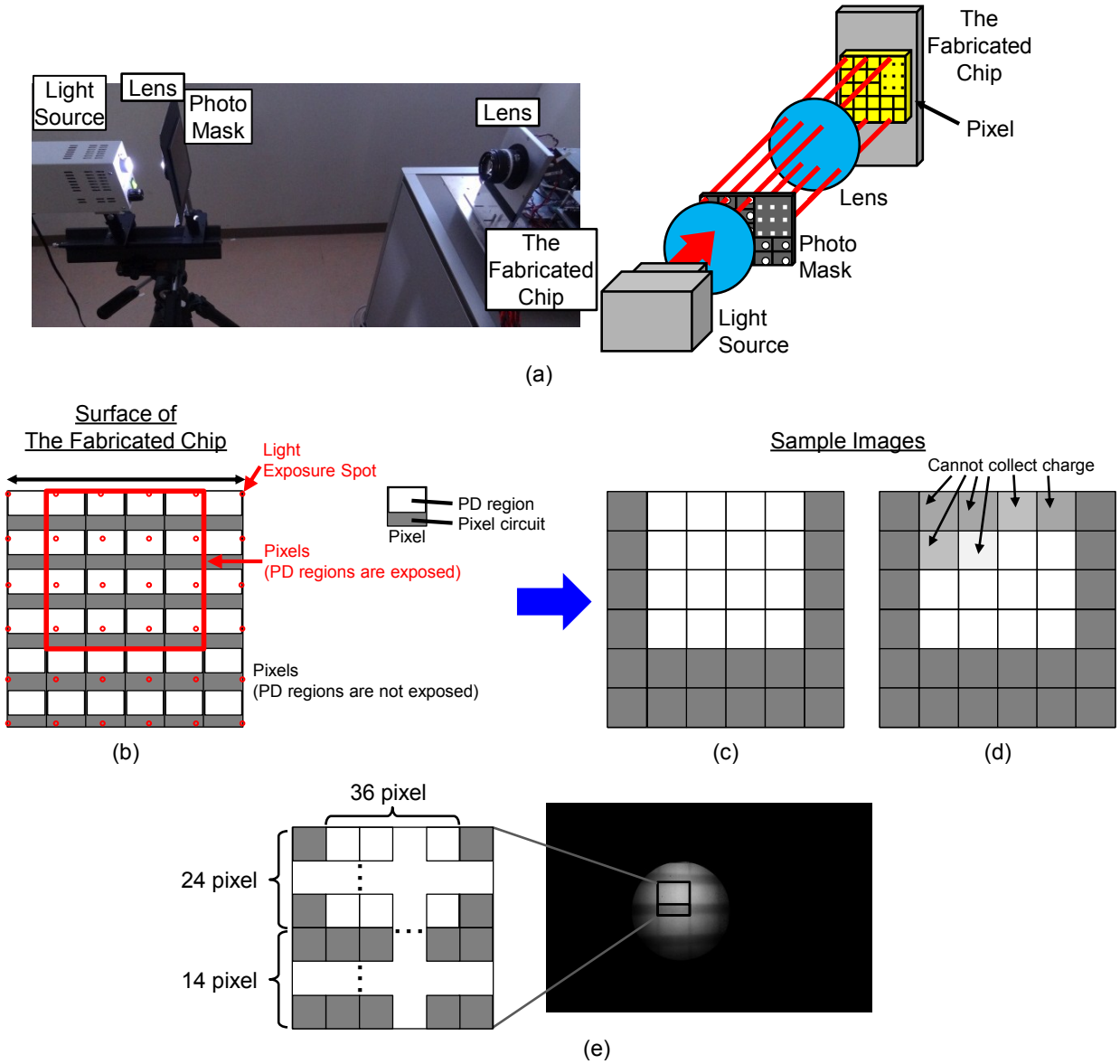


Figure 10. The measurement system and the result of sensitivity distribution in the pixel regions. (a) Measurement system, (b) pattern diagram of this experiment (light exposure spot), (c),(d) examples of the sensor outputs, (c) the case of fully charge transfer, (d) the case of not fully charge transfer, and (e) the measurement result (sample image).

3.4 Spectral response

Figure 11 shows the spectral response of the fabricated chip. This image sensor had wide spectral sensitivity from 200 nm to 1000 nm, from ultra-violet (UV) light to near infrared light. Characteristic of around 200 nm depended on that of interlayer insulators. In the UHS phenomena such as discharge phenomena, the short wavelength sensitivity near blue is required. Therefore, the fabricated chip is advantageous to capture the discharge phenomena.

3.5 Sample images

Figure 12 shows the sample images taken at 20M fps burst half resolution video operation. The object was injection of droplet from the air brush. In order to capture the droplet, we zoomed in the nozzle of the air brush with a microscope. Fig. 12 shows the sample images arranged in interval 10 frames. The images successfully captured the behavior of the droplet in detail.

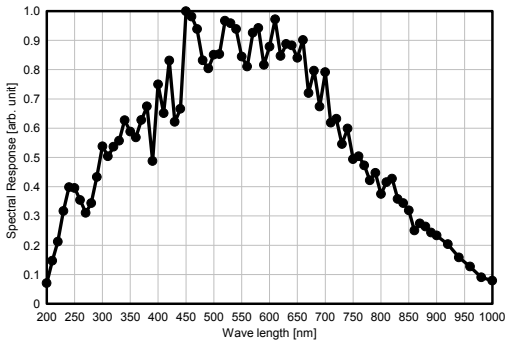


Figure 11. Spectral response of the fabricated chip.

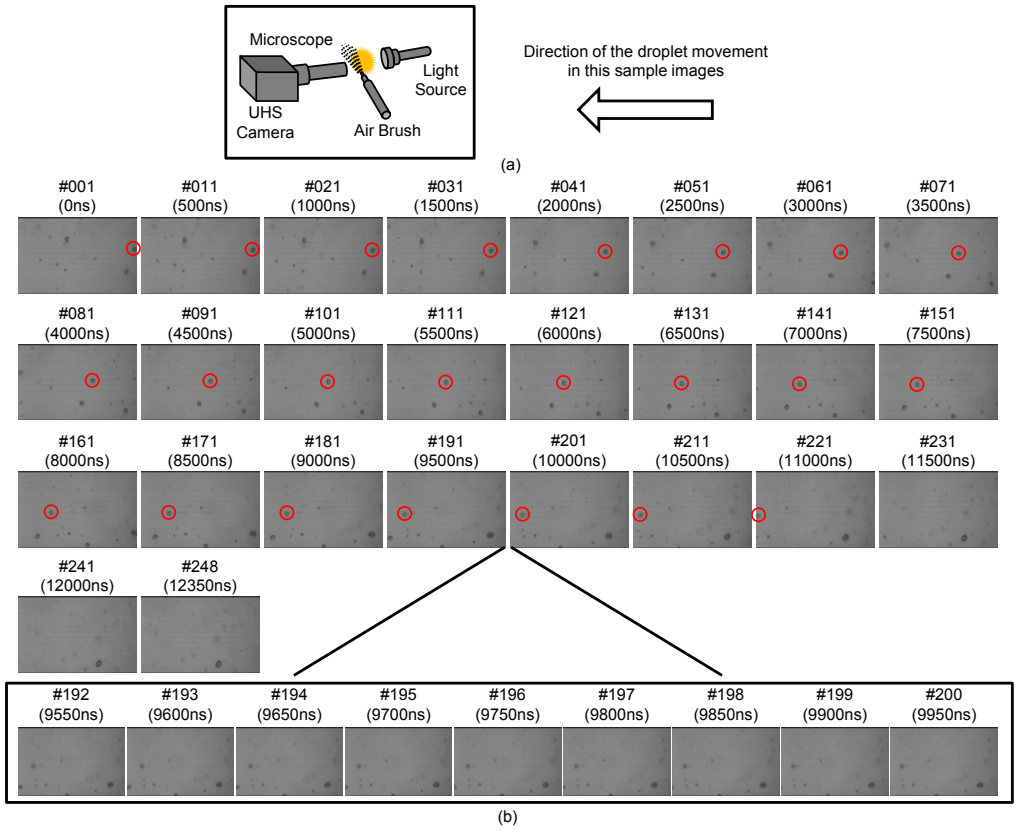


Figure 12. Sample images of the air brush injection taken at 20M fps burst half resolution video operation. (a) Measurement system, (b) sample images.

Table 2. Summary of the performance of the fabricated chip.

Image Lag	below the measurement limit	
Spectral Sensitive Range	200 nm - 1000 nm	
Fully Charge Transfer Time	≤ 10 nsec	
Mode	Full	Half
Maximum Frame Rate	10M fps	20M fps
# of Frames	128	256
Power Consumption	10W @ 10M fps	10W @ 20M fps

3.6 Performance

Table 2 shows the performance of the fabricated chip. We have already reported that maximum power consumption of the FTCMOS image sensor at 1T pixel/s was 24W [11-12]. The power consumption of the fabricated chip at 1T pixel/s was decreased to 10W because of the lower power-supply voltage.

4. CONCLUSION

In this paper, we demonstrated the technologies related to the pixel structure achieving fully charge transfer time of less than 10 nsec for the 20M fps burst CMOS image sensor. The PD size is 30.0 μm^H × 21.3 μm^V in the 32.0 μm^H × 32.0 μm^V pixel. We designed the pixel structure which included the n-layer shape and the PD dopant profile with the condition of three times n-implantation. Owing to this structure, we were able to generate an electric field greater than the average of 400 V/cm toward the FD in the entire PD region. In this pixel structure, it is possible to collect in the FD about 96 % of charges generated in the PD within 10 nsec according to the device simulation result. From the measurement result of this fabricated chip, we confirmed following performances. Image lag was less than the measurement limit. The electron transit time from the edge of the PD to the FD was about 5 nsec. The entire PD region had equivalent sensitivity. This PD had high sensitivity in the short-wavelength region as well as the long-wavelength. The power consumption of this fabricated chip at 10M fps burst full resolution and 20M fps half resolution video operation were 10 W. By using this technology, all charges generated in the large size PD are able to be collected in the FD in a short time. Therefore it is expected that this technology will be applied to many image sensors of fields such that it is necessary to collect many charges in a short time.

REFERENCES

[1] Organizers: Ramesh, T. K., Lamberson, L., Rhorer, R., Panel Members: Chen, W., Dannemann, K., Pierron, F., Reu, P., Shukla, A., Song, B., "Review of High-Rate Imaging Panel Discussion," SEM Annual Conference (2012)

[2] Sugawa, S., "Ultra-High Speed Imaging," IEEE International Solid-State Circuits Conference, Forum, Scientific Imaging (2013).

[3] Kuroda, R., Tochigi, Y., Miyauchi, K., Takeda, T., Hirose, R., Tominaga, H., Takubo, K., Kondo, Y., Sugawa, S., "Ultra-high Speed Image Sensors for Scientific Imaging," International Conference on Solid State Devices and Materials, 872-873 (2013).

[4] Etoh, G. T., Poggemann, D., Kreider, G., Mutoh, H., Theuwissen, P. J. A., Ruckelshausen, A., Kondo, Y., Maruno, H., Takubo, K., Soya, H., Takehara, K., Okinaka, T., Takano, Y., "An Image Sensor Which Captures 100 Consecutive Frames at 1 000 000 Frames/s, " IEEE Tans. Elec. Dev., 50(1), 144-151 (2003).

[5] Takeshita, H., Sawada, T., Iida, T., Yasutomi, K., Kawahito, S., "High-speed Charge Transfer Pinned-photodiode for a CMOS Time-of-Flight Range Image Sensor," Proc. SPIE 7536, 75360R-1-9 (2010).

[6] Shin, B., Park, S., Shin, H., "The effect of photodiode shape on charge transfer in CMOS image sensors," Solid-State Electronics, 54(11), 1416-1420 (2010).
[7] Crooks, J., Marsh, B., Turchetta, R., Taylor, K., Chan, W., Lahav, A., Fenigstein, A., "Ultra-high speed imaging at megaframes per second with a megapixel CMOS image sensor," Proc. International Image Sensor Workshop, 369-372 (2013).
[8] Kosonocky, F. W., Yang, G., Kabra, K. R., Ye, C., Pektas, Z., Lowrance, L. J., Mastrocola, J. V., Shallcross, V. F., Patel, V., "360 × 360 Element Three-Phase Very High Frame Rate Burst Image Sensor: Design, Operation, and Performance, " IEEE Tans. Elec. Dev., 44(10), 1617-1624 (1997).
[9] Monoi, M., Sasaki, S., Dobashi, K., Iwai, J., Sekine, H., Tomita, K., Ooki, M., Mashiko, S., Saitou, H., Itabashi, Y., "A Single Layer CCD Image Sensor with Wide Gap Electrode and Gradual Potential Channel," Proc. SPIE 7249, 72490I-1-9 (2009).
[10] Cao, Z., Zhou, Y., Li, Q., Qin, Q., Liu, L., Wu, N., "Design of Pixel for High Speed CMOS Image Sensors," Proc. International Image Sensor Workshop, 229-232 (2013).
[11] Tochigi, Y., Hanzawa, K., Kato, Y., Kuroda, R., Mutoh, H., Hirose, R., Tominaga, H., Takubo, K., Kondo, Y., Sugawa, S., "A Global-Shutter CMOS Image Sensor With Readout Speed of 1-Tpixel/s Burst and 780-Mpixel/s Continuous, " Proc. IEEE International Solid-State Circuits Conference, 382-383 (2012).
[12] Tochigi, Y., Hanzawa, K., Kato, Y., Kuroda, R., Mutoh, H., Hirose, R., Tominaga, H., Takubo, K., Kondo, Y., Sugawa, S., "A Global-Shutter CMOS Image Sensor With Readout Speed of 1-Tpixel/s Burst and 780-Mpixel/s Continuous, " IEEE J. Solid-State Circuits, 48(1), 329-338 (2013).
[13] Etoh, G. T., Nguyen, H. D., Dao, T. V. S., Vo, L. C., Tanaka, M., Takehara, K., Okinaka, T., Kuijk, V. H., Klaassens, W., Bosiers, J., Lesser, M., Ouellette, D., Maruyama, H., Hayashida, T., Arai, T., "A 16 Mfps 165 kpixel Backside-Illuminated CCD, " Proc. IEEE International Solid-State Circuits Conference, 406-407 (2011).
[14] Crooks, J., Marsh, B., Turchetta, R., Taylor, K., Chan, W., Lahav, A., Fenigstein, A., "Kirana: a solid-state megapixel uCMOS image sensor for ultra-high speed imaging," Proc. SPIE 8659, 865903-1-14 (2013).
[15] Mutoh, H., "Simulation for 3-D Optical and Electrical Analysis of CCD," IEEE Tans. Elec. Dev., 44(10), 1604-1610(1997).